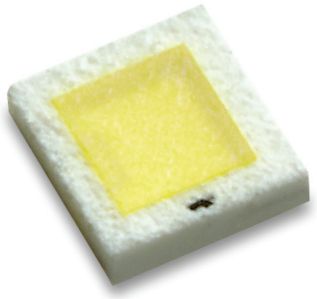
LUMILEDS

AUTOMOTIVE

LUXEON Neo 0.5mm²

Assembly and Handling Information



Introduction

This application brief addresses the recommended assembly and handling procedures for LUXEON Neo emitters. LUXEON Neo emitters are designed to deliver high luminous flux and efficacy in automotive exterior lighting applications. Due to the small size and construction, they require special assembly and handling precautions.

Proper assembly, handling and thermal management, as outlined in this application brief, ensures high optical output, long term lumen maintenance and high reliability of LUXEON Neo emitters in automotive applications.

Scope

The assembly and handling guidelines in this application brief apply to the products

- LUXEON Neo 0.5mm² CW
- LUXEON Neo 0.5mm² PCA

Any assembly or handling requirements that are specific to a subset of LUXEON Neo products is clearly marked. In the remainder of this document, the term LUXEON Neo refers to any product in the LUXEON Neo product family.

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1. Component

1.1 Reference Document

The LUXEON Neo datasheet is available upon request. Please contact your Lumileds sales representative.

1.2 Description

The LUXEON Neo emitter consists of a single LED chip combined with a phosphor converter to emit white light. It does not contain any additional carrier substrate and electrical contacts are located directly underneath the die level. The outside of the package is coated with white silicone to shield the chip from the environment and to prevent light leakage to the sides (top emitter). The LUXEON Neo emitter differs in type with and without an embedded transient voltage suppressor structure (see Table 1) in the active layers of the LED (eTVS) to protect the emitter against electrostatic discharges (ESD).

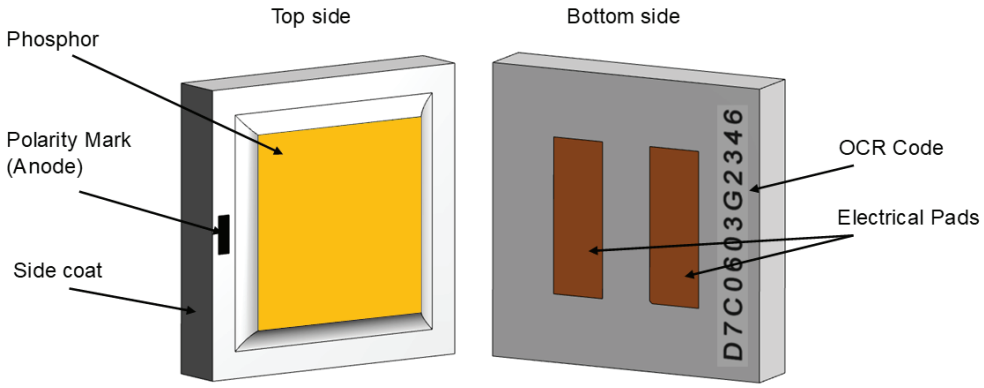
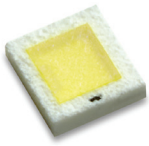
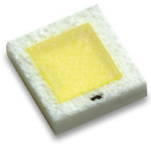
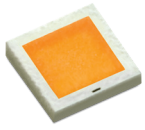


Figure 1: Top view (left) and bottom view (right) of the LUXEON Neo 0.5mm² CW

Table 1. Design features by LUXEON Neo part number

PRODUCT	PART DESCRIPTION: LUXEON NEO XXX 0.5mm²	PART NUMBER	NOMINAL DRIVE CURRENT (mA)	PACKAGE SIZE	ESD PROTECTION
	CW	A1N1-58500BH0xxxxx	500	1.13 mm x 1.13 mm x 0.253 mm	Internal TVS-structure
	CW	A1N1-58500BHNxxxxx	500	1.13 mm x 1.13 mm x 0.253 mm	External ESD protection is required
	PCA	A1N1-05910BH0xxxxx	500	1.13 mm x 1.13 mm x 0.29 mm	External ESD protection is required

1.3 Form Factor

The dimensional design for LUXEON Neo 0.5mm² is outlined below in Figure 2. See the latest LUXEON Neo datasheet for applicable tolerances.

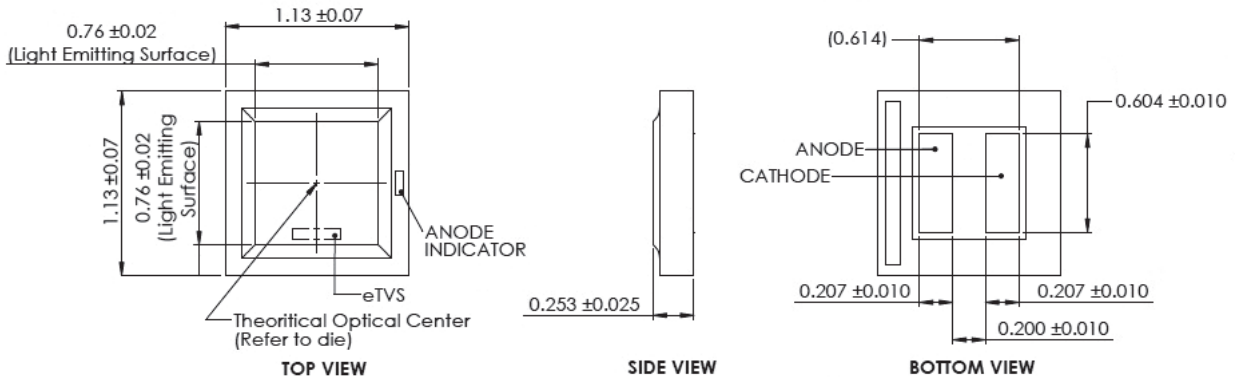


Figure 2. Dimensions in millimeters for LUXEON Neo 0.5mm²

1.4 Optical Center

The LUXEON Neo has no lens (primary optics). The optical center is at the center of the Lumiramic™ as indicated by the red dot, and the solder pad center is indicated by the green dot, both shown in Figure 3 below. The optical center to solder pad center tolerance is ±25 µm (see datasheet for latest information on tolerances). Optical rayset data of each LUXEON Neo part is available upon request.

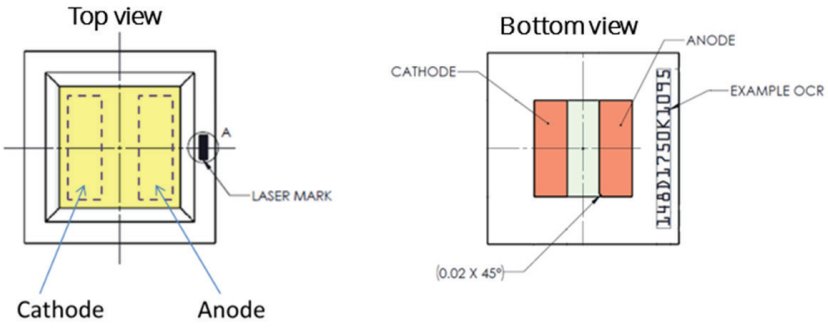


Figure 3. Theoretical optical center and solder pad center for LUXEON Neo 0.5mm²

1.5 Polarity Marking

The polarity of LUXEON Neo is marked on the top side with a black dot on the side where the anode pad is located (Top view image in Figure 4). This marking can be used during assembly setup for manual polarity verification. On the bottom anode side there is an alphanumeric OCR code (Bottom view image in Figure 4), which can be used to identify the production batch and full test parameter traceability. This marking can also be used during pick and place assembly for polarity check (see Chapter 5.7, "Vision recognition" for details).

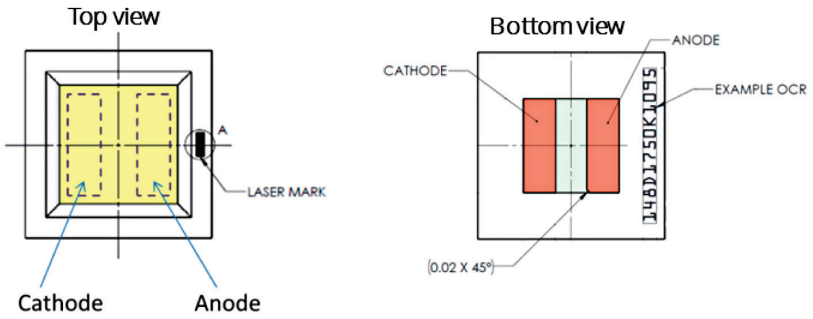


Figure 4. Top side polarity mark (left) and bottom side OCR mark (right) for LUXEON Neo 0.5mm²

1.6 Side Coat Geometry

The white side coat rim is designed to be lower than the light emitting surface (phosphor). Single particles protruding out of the side coat material may occur. At these positions, the material can be a maximum of 25 µm higher than the light emitting surface at the hatched area (see Figure 5).

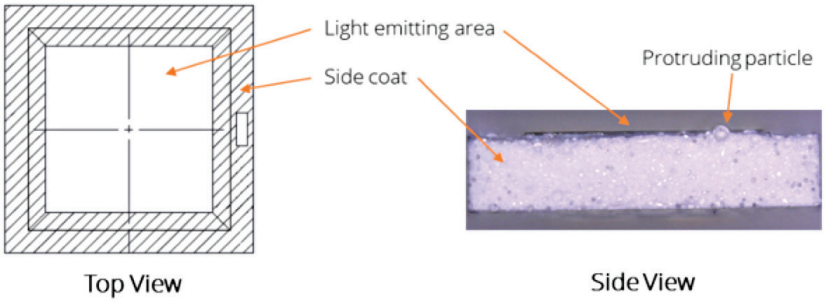


Figure 5. Side coat for LUXEON Neo 0.5mm²

The side coat represents the package outline. The center of this geometry may have an offset to the pad center and should not be used for referencing, shown in Figure 6 below (see latest datasheet for applicable tolerances).

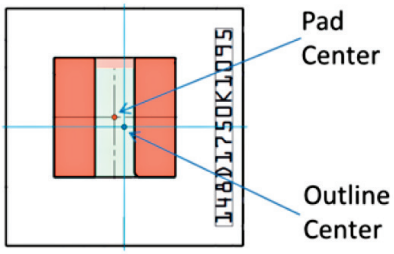


Figure 6. Offset between pad center and outline center

1.7 Mechanical Files

Mechanical drawings for LUXEON Neo (2D and 3D) are available upon request. For details, please contact your Lumileds sales representative.

2. Handling Precautions

Like all electrical components, there are handling precautions that need to be taken into account when setting up assembly procedures. These LUXEON Neo precautions are noted here in section 2.

2.1 Electrostatic Discharge Protection (ESD)

Electrostatic discharges, rapid transfers of charges between two bodies due to an electrical potential difference between those bodies, can cause unseen damage to electronic components. In LED devices, ESD events can result in a slow degradation of light output and/or early catastrophic failures. In order to prevent ESD from causing any damage, handling in a safe ESD protected environment is required and Lumileds devices without ESD protection do also require external ESD protection. See Figure 7.

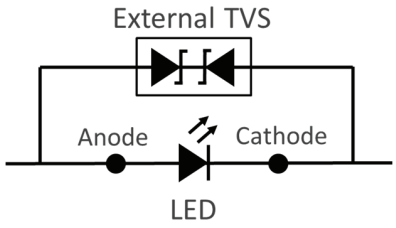


Figure 7. Example of external ESD protection for LUXEON Neo 0.5mm² without internal TVS

All in Table 1 listed types with the comment "Internal TVS-structure", include a protection diode which is parallel to the chip and in reverse direction. This embedded diode (eTVS) provides a current path for negative transient voltage (see Figure 8). Current through this eTVS structure will generate light, as well, and should not be used for normal operation. This implies that polarity check for LUXEON Neo emitters should not be done by testing light output under low current probing.

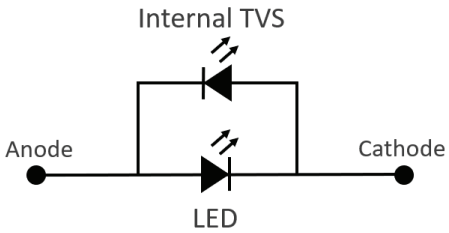


Figure 8. Example of internal ESD protection for LUXEON Neo 0.5mm² include internal TVS

Common causes of ESD include the direct transfer of charges from the human body or from a charged conductive object to the LED component. In order to test the susceptibility of LEDs to these common causes of ESD, two different models are typically used:

- Human Body Model (HBM)
- Charged Device Modell (CDM)

The LUXEON Neo 0.5 mm² CW with eTVS can according to their datasheet specifications only withstand HBM class 1C (< 2 kV) and CDM class C3 (< 500 V).

LUXEON Neo 0.5mm² CW and PCA without protection cannot achieve the lowest level of ESD standard. The factory needs to be certified to 100 V HBM to allow the assembly of LUXEON Neo. According to the datasheets the specifications are:

- CW: HBM class 0 (< 250 V) and CDM class C0a (< 125 V)
- PCA: HBM class 0 (< 250 V) and CDM class C0a (< 125 V)

Nevertheless, Lumileds strongly recommends that customers adopt handling precautions for LEDs similar to those which are commonly used for other electronic surface mount components which are susceptible to ESD events. Additional external ESD protection for the LED is needed if the LED is used in non ESD-protected environments and/or exposed to higher ESD voltages and discharge energies, e.g. as described in ISO 10605 or IEC 61000-4-2 (severity level IV). For details please contact your sales representative.

2.2 Component Handling

Minimize all mechanical forces exerted onto the silicone package of LUXEON Neo. The white package consists of fragile silicone material and should not be handled with tweezers that can lead to damage of the package, especially not with metallic tweezers. Any force above 0.5 N may damage the silicone side coat and change optical performance. A vacuum pen can be used instead of tweezers (see Figure 9).

The suction tip should be made of a soft material such as rubber to minimize the mechanical force exerted onto the top surface of the LED and apply no forces to the silicone side coat layer. Avoid contaminating the top side surface of the LED with the soft material. Do not stick any tape on top of the light emitting surface, such as capton- or UV-tape. A contamination of glue or its invisible constituent parts may change the LED performance.

Electrical testing before assembly should be avoided. Probe tips may scratch or dent the pad surface and damage active layers below. Avoid contact with the LED other than what is required for placement. Lumileds stongly recommends handling with automatic assembly equipment only where forces to the component can be well controlled.

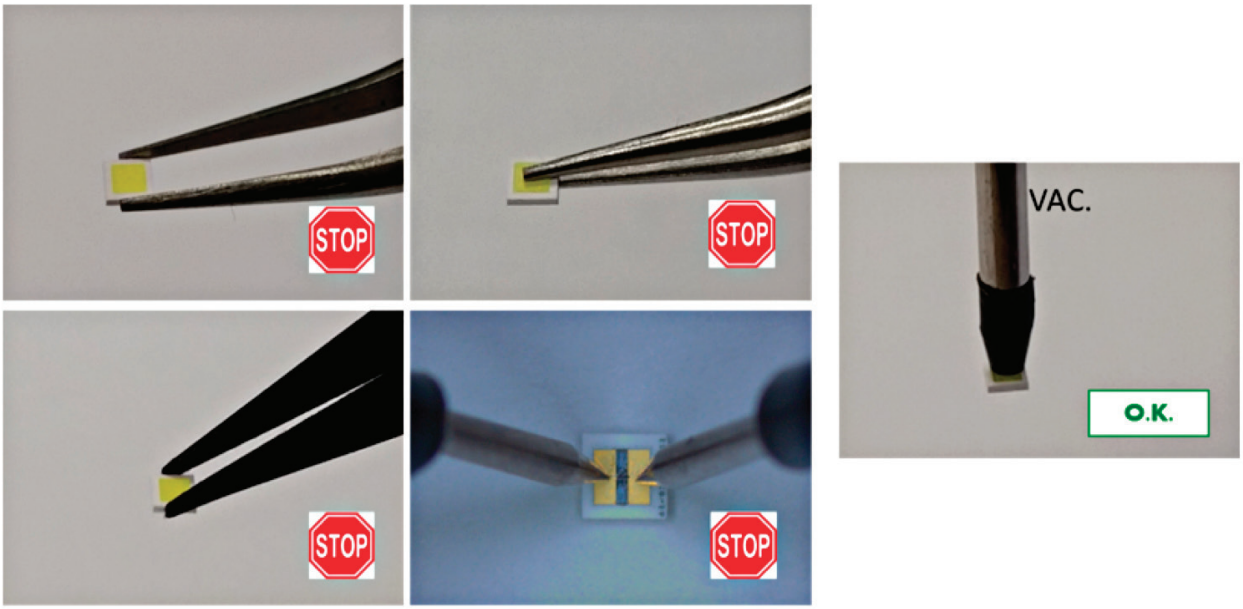


Figure 9. LED handling

Do not touch the top surface with fingers or apply any pressure to it when handling finished boards containing LUXEON Neo emitters. Do not stack finished boards because the LED can be damaged by the other board outlines. In addition, do not put finished boards with LUXEON Neo emitters top side down on any surface. The surface of a workstation may be rough or contaminated and may damage the LED.

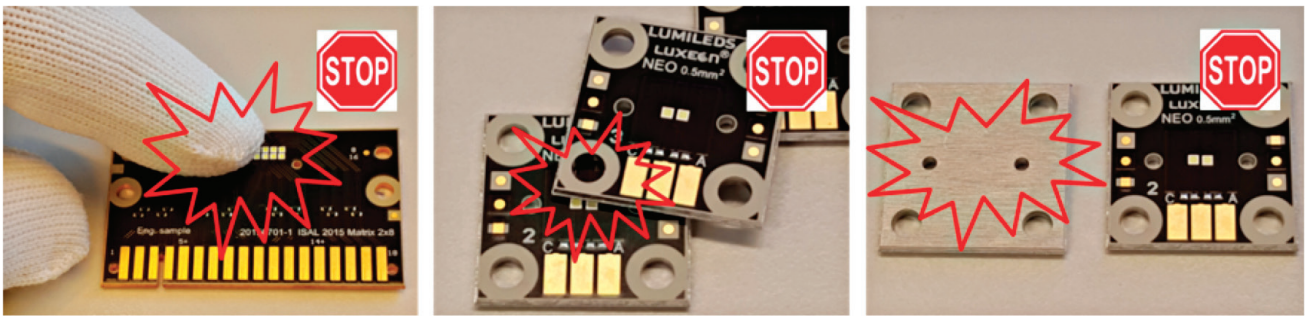


Figure 10. Board handling

Mishandling will lead to damages of side coat material shown in Figure 11 below (see Chapter 5.13 Board Handling and Bending" for proper handling of finished products).

Figure 11. Damaged LUXEON Neo emitter

2.3 Cleaning

In order to prevent any interaction between solder flux residues and the LED, Lumileds recommends a PCB cleaning step after soldering the LED, such as shown in Figure 12. E.g. a water soluble solder flux can be cleaned with deionized (DI) water. The cleaning should consist of a water spray or rinse process without applying mechanical stress to the LED. Lumileds advises against ultrasonic supported cleaning for the LUXEON Neo LED.

Figure 12. Process flow for cleaning step

The surface of the LED should not be exposed to dust and debris. Excessive dust and debris on the LED surface may cause a decrease in light output and optical behavior. It is best to keep LED in their original shipping reel until actual use.

In the event that the surface requires cleaning, a compressed gas duster or an air gun with 1.4 bar (at the nozzle tip) and a distance of 15 cm will be sufficient to remove the dust and debris. Make sure that the parts are secured first, taking above handling precautions into account.

One can also rinse with isopropyl alcohol (IPA). Do not use solvents listed in Table 9, as they may adversely react with the LED assembly. Extra care should be taken not to damage the housing around the LED chips. Lumileds does not recommend ultrasonic supported cleaning for LEDs.

3. Printed Circuit Board

3.1 PCB Requirements

The LUXEON Neo can be mounted on multi-layer FR4 Printed Circuit Boards (PCB) or Insulated Metal Substrates (IMS). To ensure optimal operation of the LUXEON Neo emitters, the thermal path between the LED package and the heatsink should be optimized according to the application requirements. Please ensure that the PCB assembly complies to the applicable IPC standards listed below.

General PCB Standards:

- IPC A-600H: Acceptability of Printed Boards
- IPC A-610F: Acceptability of Electronic Assemblies
- IPC 2221A: General Standard on Printed Board Design
- IPC 7093: Design and Assembly Process Implementation for Bottom Termination Components

Filled and Capped Via Boards:

- IPC 4761: Design Guide for Protection of Printed Board Via Structures
- IPC 2315: Design Guide for High Density Interconnects and Micro Vias
- IPC 2226: Design Standard for High Density Interconnect Printed Boards

3.2 Footprint and Land Pattern

Lumileds recommends using solder mask defined land pattern for LUXEON Neo, shown in Figure 13. Due to this, the copper area can be extended as far as possible for better heat spreading, which results in lower thermal resistance. However, a solder mask defined pad requires good mask quality and tight registration tolerances during PCB manufacturing (see Chapter 3.8 “PCB Quality” for more details).

For the solder mask defined land pattern, the self-alignment of the component during reflow soldering can be controlled well by solder mask geometry in Y-direction. To compensate the solder mask registration tolerance, the X dimension is slightly extended and the component can self-align in X-direction to the trench in the metal layer.

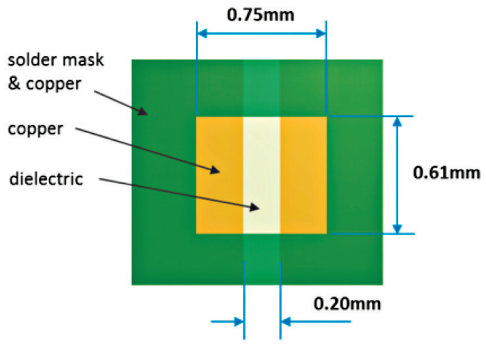


Figure 13 Solder mask defined land pattern for LUXEON Neo 0.5mm²

For applications where requirements on thermal performance are less demanding, a lower solder mask quality may be acceptable when using a metal defined pad geometry, shown in Figure 14. Self-alignment of the component during reflow is mainly defined by metal structure. The solder mask is retracted and serves to stop the solder wetting outside the LED area and it may be removed if solder wetting can be limited by solder process.

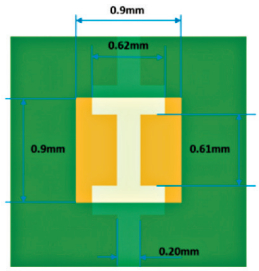


Figure 14. Metal defined land pattern for LUXEON Neo 0.5mm²

3.3 Board Fiducial for Solder Mask Defined Footprint

For the solder mask defined LUXEON Neo land pattern, an offset between metal and solder mask becomes critical during solderpaste print and SMT assembly. The component aligns according to the soldermask in Y-direction and according to metal in X-direction. In order to achieve best soldering accuracy, dedicated fiducials for LEDs can be used, which represent both layers shown in Figure 15. The shift of the shown fiducial is defined by soldermask in Y-direction and by metal in X-direction, identical to the shift of the LED. The fiducial must be aligned in the same orientation as the LEDs. The vision recognition in the SMT process must be programmed to detect the exposed metal square of 1mm x 1mm. A dark solder mask color may be needed for proper contrast.

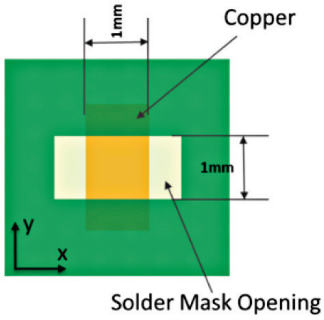


Figure 15. Solder mask and metal defined fiducial

3.4 Array Configuration

For applications that require low position tolerances between multiple LEDs, they should be oriented in the same direction. Avoid 90 degree rotation within this array. Spacing of LEDs down to 0.2 mm edge-to-edge for high density needs is feasible, assuming capable processes. A spacing of 0.3mm or more is prefered to avoid mechanical contact.

3.5 Surface Finishing

Lumileds recommends using ENIG (Electroless Nickel Immersion Gold) plating according to IPC-4552. Other surface finishes are possible but have not been tested by Lumileds. Surface finish Hot-Air-Solder-Leveling (HASL) may have inhomogenious pad height and is not recommended for LUXEON Neo.

3.6 Solder Mask

A solder mask thickness of 21 µm ±7 µm on top of metal layer is desired. Mask and PCB vendors have to be evaluated for proper quality. Systems with a photo lithographic structuring process are known to deliver better tolerances than screen printed materials. Due to the small footprint of the LUXEON Neo emitters, this requirement is important in order to achieve good assembly quality.

3.7 Silk Screen or Ink Printing

Silk screen markings within and around the LUXEON Neo outline should be avoided because the height of the ink may interfere with the LUXEON Neo and solder stencil printing process. This can cause rotation, tilt and increased risk of solder bridging (short circuit). If needed, the ink printing should be at least 2 mm away from the LUXEON Neo outline.

3.8 PCB Quality and Supplier

Select only PCB suppliers that are capable of delivering the required level of quality. Leastwise, the PCBs must comply with IPC standard IPC-A-600H, 2010 (“Acceptability of Printed Boards”).

A maximum mask registration tolerance of 50 µm between the copper trace pattern and solder mask is desirable to achieve optimum solder joint contact area using the recommended solder mask defined footprint as shown in Figure 13. If the offset between the solder mask and the copper land pattern is large, one side of electrode pads will have less solder joint contact area. This may affect package centering, tilting, and thermal performance and may increase risk of solder bridging (short circuit) and solder balling if the stencil is not properly aligned to the solder mask during printing.

Figure 16 shows an example of the solder pad size for three different registration offset levels between the copper trace pattern and the solder mask for LUXEON Neo 0.5mm² using the recommended footprint in Figure 13. Large misalignment between solder mask opening and copper trace will cause one of the two copper land patterns to be smaller than the other. Depending on the PCB manufacturer capability, PCB cost consideration and customer position tolerance needs, it may be necessary to extend the area of the solder mask opening.

Figure 16. Solder mask registration offset to copper trace

4. Thermal Management

4.1 Thermal Resistance

The thermal resistance between the junction of the LED and the bottom side of the PCB depends on the following key design parameters of a PCB:

- PCB dielectic materials
- Cu plating thickness
- Solder pad pattern and solder thickness
- Distance to neighbogring heat source (LED spacing)

Lumileds conducted simulations to evaluate the thermal performance of LUXEON Neo on different PCB design concepts. Details of the simulation model are given in Figure 17. The model geometry comprises the LUXEON Neo on a board (Cu-IMS or FR4 board) that is mounted on a plate Al heatsink. A thermal interface material (TIM) is assumed between board and heatsink. The impact of different top-side Cu patterns, as shown in Figure 17, was investigated for the Cu-IMS boards. Here, pattern 1 represents a solder mask defined layout, whereas pattern 2 uses metal-defined pads in *y*-direction. The thermal resistances junction-to-board bottom $R_{th,j\text{-}b,el}$ (thermal resistance based on electrical input power) are calculated as $R_{th,j\text{-}b,el} = R_{th,j\text{-}b,real}/(1–WPE)$, where WPE denotes the "wall plug-in efficiency." The WPE is not constant and depends on drive condition and flux binning class. The thermal resistance $R_{th,j\text{-}b,real}$, based on thermal power, is obtained by $R_{th,j\text{-}b,real} = (T_j\text{-}T_b)/P_{th}$ using the average junction temperature, T_j, and the maximum temperature at the bottom side of the board, Tb, obtained from the simulations along with the thermal input power P_{th}.

Simulation Details

Simulation Model

- Neo on board and plate heat sink with TIM
- Heat conduction only
- Bottom of heat sink is assumed to be ideally heat-sunk to ambient

Heat Sink and TIM Parameters

- Heat sink size: 50 mm x 50 mm x 10 mm
- Heat sink material: Al – 150 W/(mK)
- TIM thickness: 100 µm
- TIM th. cond.: 1 W/(mK)

Solder Parameters

- Thickness (BLT): 50 µm
- Th. conductivity: 56 W/(mK)

Board Parameters

- Board area: 20 mm x 20 mm
- Board thickness: 1.0 mm (Cu-IMS) or 1.2–1.5 mm (FR4)
- Cu layer thickness: 35 µm or 70 µm
- Solder mask: 20 µm
- IMS diel. thickness: 100 µm, 75 µm, or 38 µm

Board Thermal Conductivities

- Cu: 390 W/(mK)
- IMS dielectric: 1.4 W/(mK), 2.2 W/(mK), or 3 W/(mK)
- FR4 epoxy: 0.3 W/(mK)
- Vias plating: 390 W/(mK)
- Vias filling: 0.3 W/(mK)

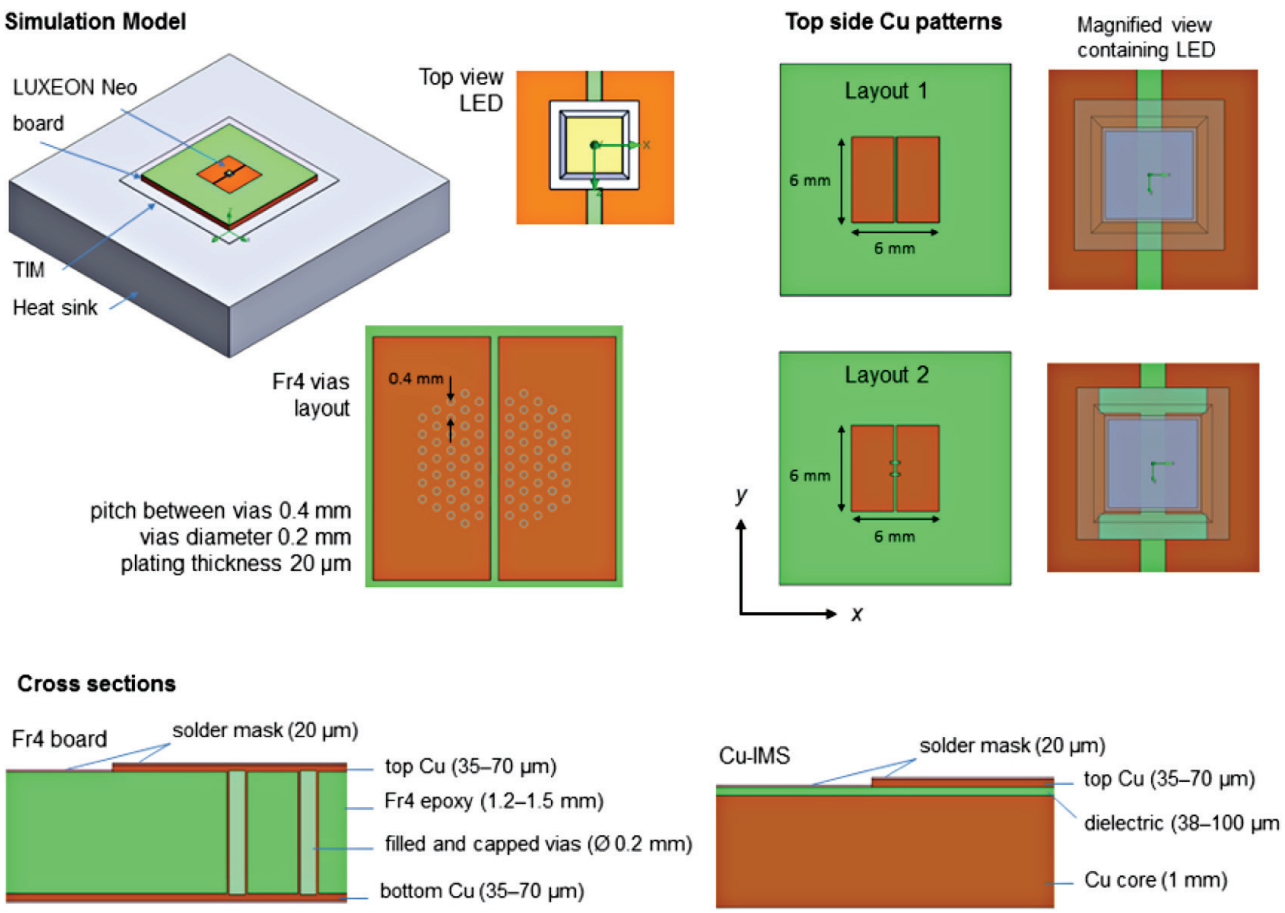


Figure 17. Geometry and board parameters used in the simulations

Simulation Results

Lumileds' recommendation to optimize the thermal performance of the system is to use a Cu-based metal-core board with a thermally well performing dielectric. The simulated thermal resistances ($R_{th,j\text{-}b,el}$) for different boards are given in Table 2 below. The values are based on electrical input power assuming an optical efficiency (WPE) of 0.3.

Table 2. Simulated LED-juntion-to-board-bottom thermal resistances ($R_{th,j\text{-}b,el}$), assuming a WPE of 0.3, for different board types

BOARD MATERIAL AND DIELECTRIC	TOP-SIDE Cu LAYOUT #	TOP Cu 35 µm	TOP Cu 70 µm
		$R_{th,j\text{-}b,el}$	
1.5 mm FR4 with filled and capped vias	1	20.9 K/W	16.3 K/W
1.2 mm FR4 with filled and capped vias	1	20.4 K/W	15.7 K/W
1.0 mm Cu-IMS, 3 W/(mK) – 38 µm dielectric	1	14.1 K/W	12.2 K/W
	2	15.8 K/W	13.6 K/W
1.0 mm Cu-IMS, 2.2 W/(mK) – 75 µm dielectric	1	16.6 K/W	13.8 K/W
	2	19.9 K/W	15.9 K/W
1.0 mm Cu-IMS, 1.4 W/(mK) – 100 µm dielectric	1	18.9 K/W	15.2 K/W
	2	24.2 K/W	17.8 K/W

4.2 Close-Proximity Thermal Performance

For small distances between the individual LEDs, thermal crosstalk can occur, leading to enhanced junction temperatures. Lumileds recommends using thermally well performing boards like Cu-IMS with high-conductivity dielectric to optimize the thermal performance.

Lumileds conducted thermal simulations of 1x2, 1x3, and 2x3 LED arrangements of different pitches as schematically shown in Figure 18. The thermal resistances ($R_{th,j\text{-}b,el}$) are given in the graphs in Figure 18. The same power was assigned to all the LEDs in the simulations and the $R_{th,j\text{-}b,el}$ values are based on the situation where all LEDs are switched on. An optical efficiency of 0.3 was assumed to calculate $R_{th,j\text{-}b,el}$. As the individual LEDs reach different temperatures, depending on their position within the array, different $R_{th,j\text{-}b,el}$ values are indicated for the outer and the center LEDs of the array. These values have been calculated using the average junction temperature of the individual LED and the electrical power of the individual LED. It can be seen that the $R_{th,j\text{-}b,el}$ values referring to the center LEDs are higher than those referring to the outer LEDs, indicating higher junction temperatures for the LEDs in the center. Note that the point of maximum board bottom temperature can shift depending on the spacing between the LEDs and position of the LEDs with respect to the board edges, which can cause a slightly non-monotonic behavior of the curves.

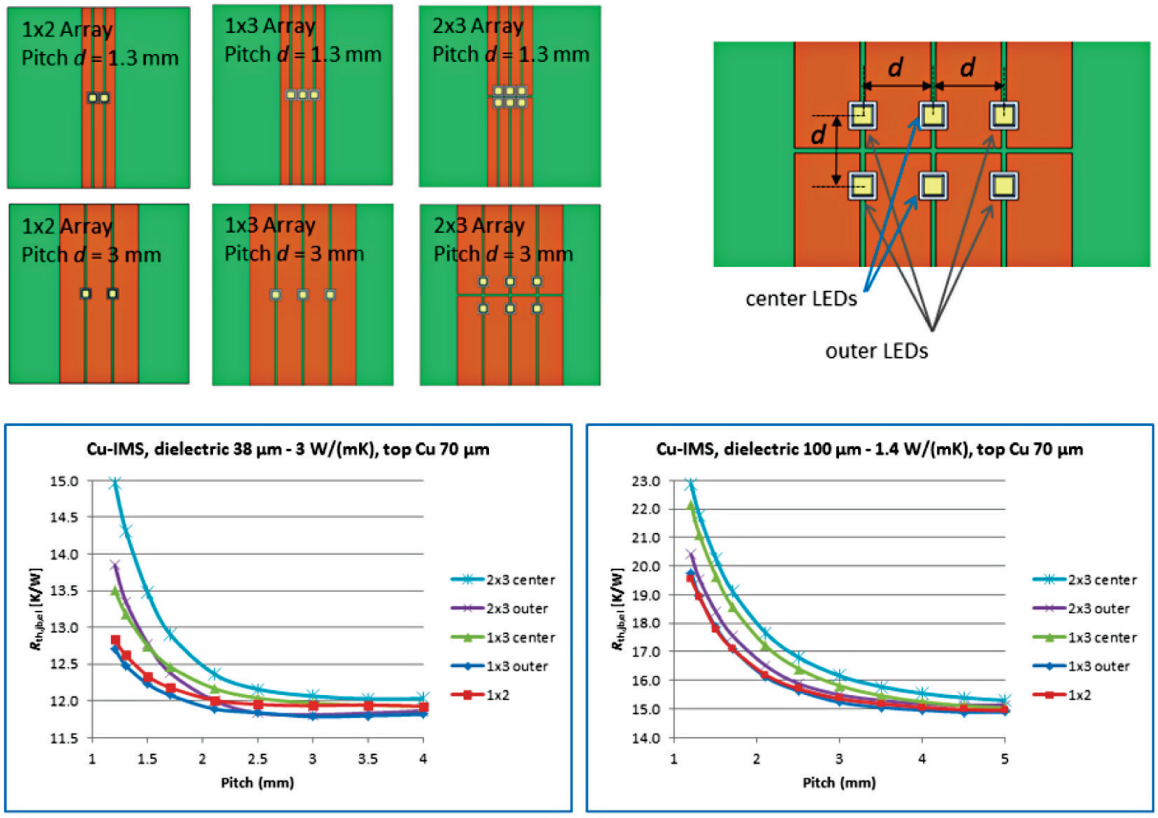


Figure 18. Top: 1x2, 1x3, and 2x3 array configurations with different pitch *d* between the LEDs; Bottom: Simulated $R_{th,j\text{-}b,el}$ of the individual LEDs within the array

4.3 Thermal Measurement Instructions

The use of a temperature probe may be desirable to verify the overall system design model and expected thermal performance. Depending on the required temperature measurement accuracy, different methods are possible to determine the LED temperature in terms of case temperature (T_c). They are listed in Table 3 and enable an indirect measurement of T_c. The more accurate the measurement is, the closer T_c can be designed to the maximum allowable T_c as specified in the LUXEON Neo datasheet. Figure 17 schematically shows the LED soldered to a PCB, including the relevant temperatures as defined for specific positions in the setup.

Table 3. Temperature measurement methods

METHOD	ACCURACY (°C)	EFFORT	EQUIPMENT COST
Thermo sensor (e.g. thin wire thermocouple)	±2.0 – ±5.0 [1]	Low	Low
Forward voltage measurement	±0.5	High	High
Infrared thermal imaging	±2.0 – ±10.0 [2]	Medium	High

Notes for Table 3:
1. See section "Temperature Probing by Thermo Sensor" for parameters determining the measurement accuracy.
2. See section "Temperature Measurement by IR thermal imaging" for parameters determining the measurement accuracy.

Temperature Probing by Thermo Sensor

A practical way to verify the case temperature (T_c) is to measure the temperature T_{sensor} on a predefined sensor pad thermally close to the case by means of a thermocouple or a thermistor as shown in Figure 19. The solder mask must be removed to ensure good thermal contact of the thermocouple to the board and to obtain accurate readings. In case of an unsymmetrical layout, T_{sensor} should be placed at the pad of higher thermal impedance. In order to get a large signal, it is recommended using the highest possible drive current for the application.

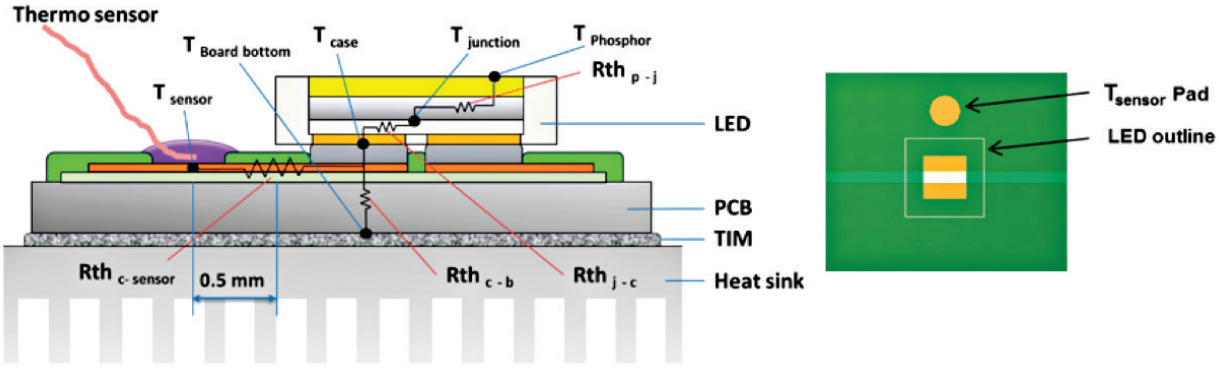


Figure 19. Temperature probing (schematically)

The case temperature (T_c) can be calculated according to the following equation:

$$T_c = T_{sensor} + R_{th,c\text{-}sensor,el} \times P_{electrical}$$

In this equation, T_{sensor} is the sensor temperature at the predefined location and Pelectrical is the electrical power of the LUXEON Neo emitters. The thermal resistance ($R_{th,c\text{-}sensor}$) is application-specific and can be determined with help of thermal simulations and measurements. Lumileds has determined the typical $R_{th,c\text{-}sensor,el}$ for LUXEON Neo on different board types (see table 2). Here, the sensor has been mounted at a distance of 0.5mm to the edge of the package. The accuracy of the measurement depends on the board type, the measurement accuracy of the thermocouple and the mounting position. The temperature signal at the thermocouple measurement point is higher for boards with large heat spreading in the top Cu layer (typically boards with large top Cu thickness and less conductive dielectric). LED boards with different configuration, design or material than given in Table 2 may require additional thermal modeling or measurments to determine the right $R_{th\ c\text{-}sensor,el}$. Please refer to section "Thermal Resistance" of this document for more detailed information regarding the design parameters.

The Lumileds Application Support team offers support to determine $R_{th,c\text{-}sensor,el}$. Please contact your Lumileds sales representative.

Table 4. Typical $R_{th,c\text{-}sensor,el}$ values of different board concepts

BOARD TYPE	$R_{th,c\text{-}sensor,el}$
IMS with dielectric of 3 W/(mK), 38 µm thickness, 70 µm Cu	10 K/W
IMS with dielectric of 2.2 W/(mK), 75 µm thickness, 35 µm Cu	13 K/W

Temperature Probing by Forward Voltage Measurement

The forward voltage measurement uses the temperature dependency of the LEDs forward voltage. The forward voltage, after switching off the thermally stabilized system, is measured and analyzed, yielding information on the LED junction temperature. By using a thermal model of LUXEON Neo or the LED junction-to-case thermal resistance, as indicated in the datasheet, the case temperature (T_c) can be estimated. To ensure high accuracy, a precise and fast voltage measurement system is needed. In addition, the relationship between forward voltage (V_f) and temperature needs to be properly characterized for each individual LED. Please contact your Lumileds sales representatives for further support in this topic.

Temperature Probing by Infrared Thermal Imaging

Infrared (IR) thermal imaging can be used to measure the surface temperature/phosphor temperature of the LED or the board temperature. For an accurate determination of the absolute temperature, the determination of the exact emissivity value is crucial. The emissivity generally depends on material, surface properties and temperature. It can be determined by heating up the unbiased device to a defined temperature that can be, for example, measured with a thermocouple. Then, an IR measurement can be taken of this setup, and the emissivity setting of the material of interest (typcially the phosphor or the board surface) can be adjusted to match the thermocouple reading. The obtained emissivity value can be used to evaluate the IR image of the device in operation to determine the temperature of interest. The temperature at which the emissivity value is determined should be similar to the temperature in operation that is to be measured. During IR imaging, make sure that the recorded image is not disturbed by unwanted background reflections. Due to the small dimensions of the LUXEON Neo, an imaging system with high magnification should be used in order to get a sufficient resolution of the LED in the IR image.

Note that due to losses in the phosphor converter layer, the phosphor temperature is typcially higher by up to 5 °C than the LED junction temperature.

5. Assembly Process Recommendations and Parameters

5.1 Solder Paste

For reflow soldering, a standard lead free SAC solder paste (SnAgCu) with no clean flux can be used. The majority of the Lumileds internal testing has been conducted with the Indium 8.9HF SAC305 solder paste, which showed reasonable reflow and voiding performance for the given settings. Solder paste with powder type 3 is recommended for required stencil thickness and aperture size.

5.2 Stencil Design

For solder mask defined land pattern, the appropriate stencil aperture is given in Figure 20. The corner radius of stencil aperture should be selected according to paste particle size to improve paste release. For type 4 paste, a radius of 50 µm is recommended.

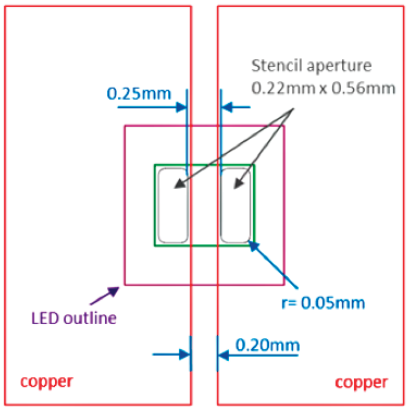


Figure 20. Stencil aperture design for LUXEON Neo 0.5mm²

5.3 Stencil Printing

The recommended stencil thickness for LUXEON Neo 0.5mm² is 3 mils (75 µm). It may be necessary to make some adjustments to the stencil thickness (for example, with the use of thicker solder mask or the presence of other components where stencil thickness is critical to that component) and aperture to optimize quality of the solder joint under customer's own assembly process. Several important factors need to be considered for obtaining good quality stencil printing (see Figure 21). They are:

1. The aperture (stencil opening) wall should be smooth, free of debris, dirt, and/or burrs, and have a uniform thickness throughout the stencil plate. Electro-polishing or nano-coating the aperture walls can aid smooth release of solder paste.
2. Positional tolerance between the stencil plate and the PCB substrate must be small enough to ensure that the solder paste is not printed outside the pad area. Hence, both the stencil plate and the PCB must be secured properly.
3. Solder mask thickness and flatness has an impact on print quality.
4. During solder paste printing, the stencil plate must be flush with the top of the solder mask. Large particles between the stencil plate and PCB may prevent a good contact (e.g. automatic stencil cleaning).
5. The PCB substrate must be mechanically supported from the bottom to prevent flexing of the PCB during solder paste printing.

Using an automatic stencil printing machine with proper fiducials or guiding feature on the PCB and the stencil plate will yield the best accuracy and repeatability for the solder paste deposition process. A manual stencil printing process is not recommended for the small pad features of LUXEON Neo mm².

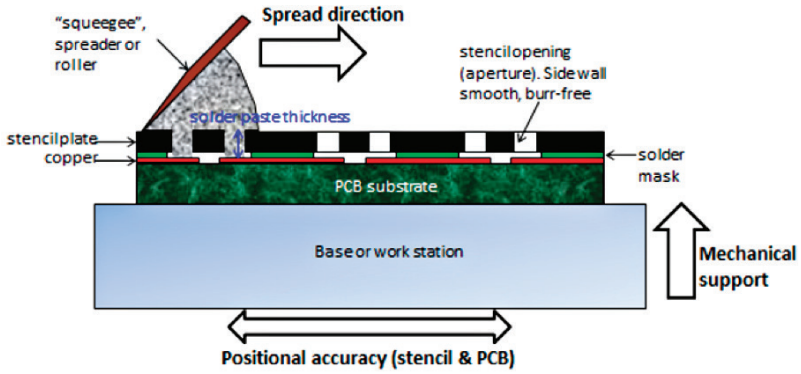


Figure 21. Stencil printing process

Figure 22 shows some examples of good and bad solder paste printing processes. A good reference to acceptable solder paste printing criteria can be found in the IPC-7527 "*Requirements for Solder Paste Printing*" document. If the solder paste print process is in control, the dimensions of the solder paste on the PCB after print will match the size of the stencil opening. Stencil printing direction should follow the long side of the pads to ensure that the stencil opening is being completely filled with solder paste and equal size. Avoid print direction along the short side of the pads (see Figure 23).

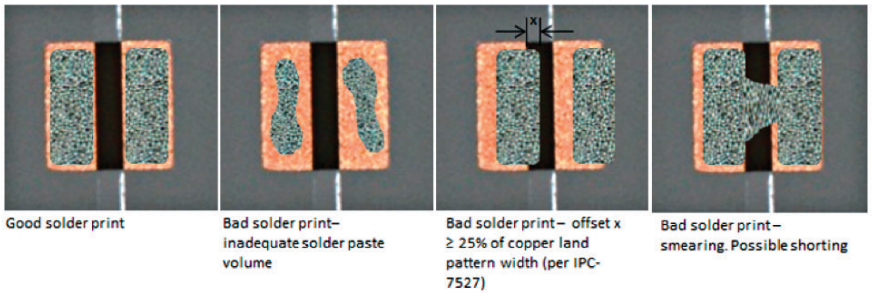


Figure 22. Example of good and bad solder paste printing

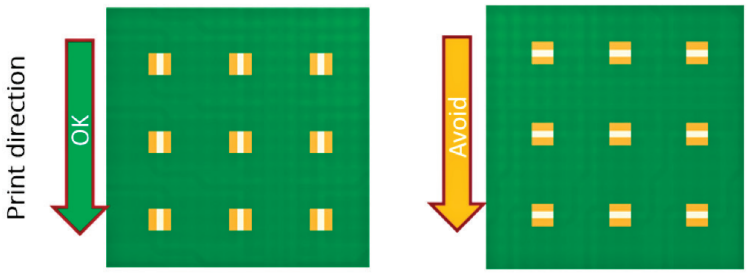


Figure 23. Orientate the PCB such that the stencil printing direction is along the long side of the pads

5.4 Pick and Place Nozzle

The LUXEON Neo is packed in a tape and reel with the light emitting surface facing upwards. Automated pick and place equipment provides the best handling and placement accuracy for LUXEON Neo emitters.

Lumileds recommends taking the following general pick and place guidelines into account:

1. The pick-up area is defined in Figure 24.
2. The nozzle tip should be clean and free of any particles since this may interact with the top surface coating of the LUXEON Neo during pick and place.
3. During setup and the first initial production run, it is good practice to inspect the top surface of LUXEON Neo emitters under a microscope to ensure that the emitters are not accidentally damaged by the pick and place nozzle.
4. To avoid any mechanical overstress, it is a good choice to use soft material for pickup; rubber nozzles are available from various suppliers.
5. Ceramic nozzle can be used for low mass nozzles.
6. Lower Z-axis velocity at the point of board contact to avoid LED damage.

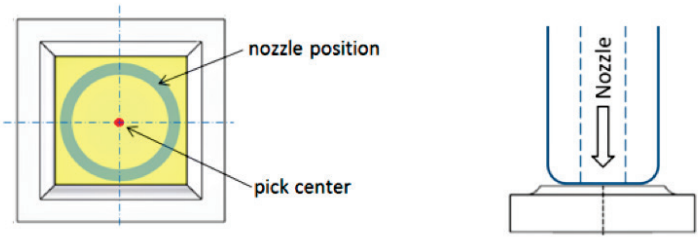


Figure 24. Pick-up area for LUXEON Neo

Since LUXEON Neo has no primary optics or lens which can act as a mechanical enclosure protection for the LED chip, the pick-up and placement force applied to the top of the package should be minimized and kept well controlled.

Picking the component out of the carrier tape should be performed from a defined height position and should not apply forces to the component and carrier tape, as this may damage the component. The LUXEON Neo is packed in a recess of the carrier tape, and the nozzle geometry must be selected accordingly to not get in contact with carrier tape (see Figure 25).

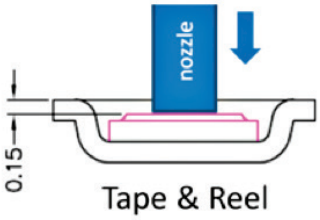


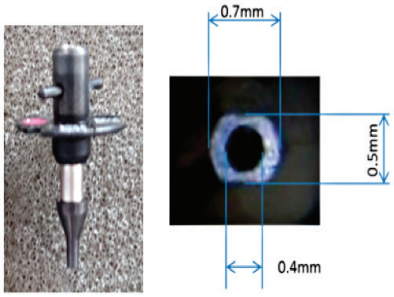
Figure 25. Pick-up from carrier tape

Standard Nozzle

Figures 26 and 27 show the standard pick and place nozzle designs for different SMT machine vendors, which can be used to handle the LUXEON Neo emitters.

Vendor	ASM Siplace
P&P Head	CPP / CP20 / CP20P
Type	2003 / 1003 / 4103
Material	Ceramic
D-outer	0.9mm x 0.5mm

Figure 26. ASM Siplace nozzle recommendation for LUXEON Neo 0.5mm²



Vendor	Fuji
Type	AA735
Material	Ceramic
D-outer	0.7mm x 0.5mm
D-inner	0.4mm

Figure 27. Fuji machine nozzle recommendation for LUXEON Neo 0.5mm²

Nozzles for specific equipment platforms are under analysis. Please contact your Lumileds sales representative if you need support regarding pick and place nozzle selection.

5.5 Placement Force / Height Control

In order to avoid any damage of the LED and minimize squeeze-out of solder paste, placement process needs to be tightly controlled. Lumileds recommends using low placement forces or a Z-height controlled placement during the pick and place process. The force during pick and place should not exeed 1.0 N. An additional large dynamic peak force occurs if the LED is placed with high Z-axis velocity at the point of touching the board and if the nozzle mass is high. Under worst case conditions, the phosphor or the sensitive LED side coat can be damaged if, for example, large particles are underneath or, due to a placement offset, the side coat touches the board surface (see Figure 28). Lower the Z-axis velocity if needed.

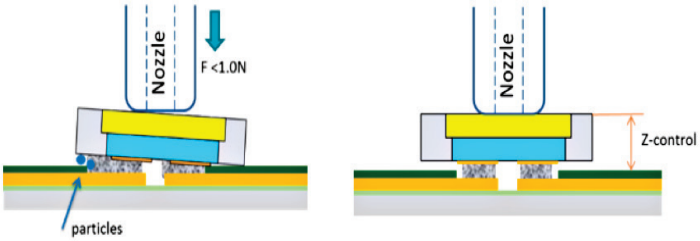


Figure 28. Placement control

5.6 Feed System

Pick and place machines are typically equipped with special pneumatic or electric feeders to advance the tape containing the LEDs. The indexing step in the pick and place process may cause some LEDs to accidentally jump out of the pocket tape or may cause some LEDs to get misaligned inside the pocket tape, resulting in pick-up errors. Depending on the feeder design, minor modifications to the feeder can substantially improve the overall pick and place performance of the machine and reduce/eliminate the likelihood of scratch or damage to the LEDs. Optimum situation will be given when the pickup position is right after cover tape peel off. Do not leave index positions uncovered between peel off and pick position. This will prevent the LEDs from tilting over or jumping out when indexing. Also, the cover tape peeling angle, relative to the tape, should be small to reduce the vertical pulling force during indexing (see Figure 29).

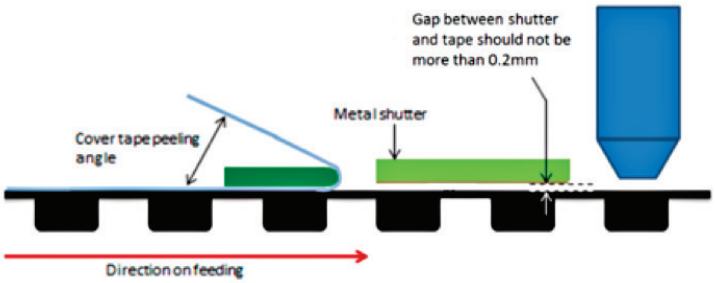


Figure 29. Pick position and cover tape peeling

5.7 Vision Recognition

For component alignment in pick & place machine, Lumileds recommends using bottom view pattern recognition. The package outline should not be used as placement reference, because there can be a significant offset between pad center and outline center (see latest datasheet for applicable tolerances). During bottom view pattern recognition, the electrical pads of LUXEON Neo should be used for alignment. Laser alignment of component outline in SMT assembly is not suitable.

Light settings are important for pads to be detectable. A coaxial lighting shows best contrast, and search algorithm can detect inner pads as placing reference (see Figure 30). A high resolution of the vision system is required for proper alignment, and a resolution of 15 µm/pixel or less is desirable.

The visibility of inner dark trench between the solder pads may change depending on overflow of white side coat material (see Figure 30). This is a normal condition and the inner geometry cannot be used for proper component alignment.

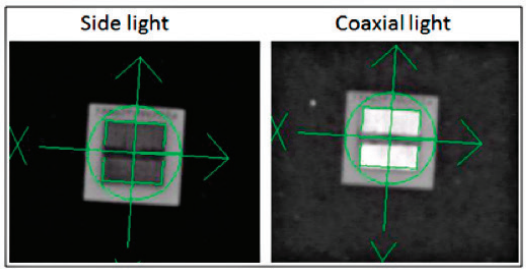


Figure 30. Bottom vision for different light settings

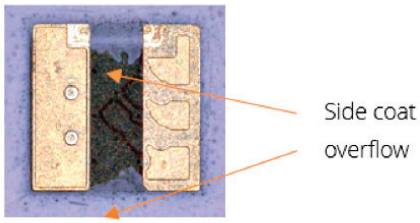


Figure 31. Side coat between pads

Polarity Check

During automated pick and place, the polarity could be checked before placing the component on the board, if required. The laser mark on the bottom side (OCR code) can be used as polarity mark for this. It is marked at the anode side of the LED. The light settings need to be adjusted in order to give good contrast. Modern SMT machines can recognize this by measuring the grey level in a defined area or comparing the grey level between two measurement areas to deliver more reliable results (see Figure 32).

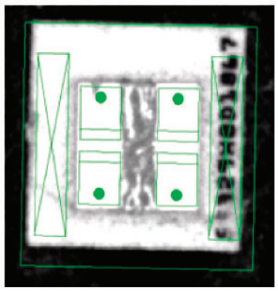


Figure 32. Automatic polarity recognition

5.8 Placement Accuracy

In order to achieve the highest placement accuracy, Lumileds recommends using an automated pick and place tool with a vision system that can recognize the bottom metallization of a LUXEON Neo. Placement accuracy of used automated equipment should be less than ±40 µm according to IPC9850A.

5.9 Reflow Profile

The LUXEON Neo is compatible with standard surface-mount and lead-free reflow technologies. This greatly simplifies the manufacturing process by eliminating the need for adhesives and epoxies. The reflow step itself is the most critical step in the reflow soldering process and occurs when the boards move through the oven and the solder paste melts, forming the solder joints. To form good solder joints, the time and temperature profile throughout the reflow process must be well maintained.

A temperature profile consists of three primary phases:

1. Preheat: the board enters the reflow oven and is warmed up to a temperature lower than the melting point of the solder alloy.
2. Reflow: the board is heated to a peak temperature above the melting point of the solder, but below the temperature that would damage the components or the board.
3. Cool down: the board is cooled down rapidly, allowing the solder to freeze, before the board exits the oven.

As a point of reference, the melting temperature for SAC 305 is 217 °C, and the minimum peak reflow temperature is 235 °C.

Lumileds successfully utilized the reflow profile in Figure 33 and Table 5 for LUXEON Neo on MCPCB.

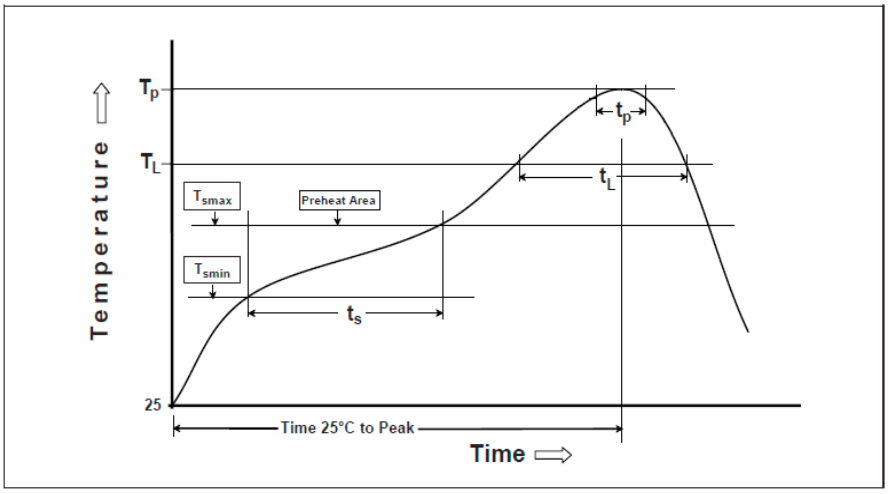


Figure 33. Reflow profile definition according to JEDEC J-STD-020E

Table 5. Temperature measurement methods

PROFILE FEATURE	MINIMUM VALUE	TYPICAL VALUE FOR SAC	MAXIMUM VALUE
Preheat Minimum Temperature (T_{smin})		150 °C	
Preheat Maximum Temperature (T_{smax})		200 °C	
Ramp-Up Rate (T_L to T_p)		2 °C / sec. avg.	3 °C / second
Preheat Time (t_{smin} to t_{smax})		100 seconds	120 seconds
Liquidus Temperature (T_L)		217 °C	
Time Maintained Above Temperature T_L (t_L)		60 seconds	120 seconds
Peak / Classification Temperature (T_p)		240 °C	260 °C
Time Within 5 °C of Actual Peak Temperature (t_p)	10 seconds	20 seconds	
Time Within 5 °C of Maximum Peak Temperature			30 seconds
Ramp-Down Rate (T_p to T_L)		2.5 °C / sec. avg.	6 °C / second
Time 25 °C to Peak Temperature	240 seconds	310 seconds	480 seconds
Nitrogen Atmosphere (O2)		<1000ppm	

Note: All temperatures refer to the application Printed Circuit Board (PCB), measured on the surface adjacent to the package body.

Things to watch for after reflow should include:

1. Solder voids—perform x-ray inspection (see Chapter 5.10)
2. Solder bridge between anode and cathode
3. Solder balling
4. Any visible damage, tilt or misplacement of LUXEON Neo
5. Any contamination on light emitting area—this may impact the light output extraction or cause color shift
6. Functional test (open/short)

5.10 Void Inspection

A large percentage of voids in the thermal path or bad solder wetting will increase the thermal resistance. An inline X-ray machine can be used to inspect voids or solder defects after solder reflow. Figure 34 shows examples of good and bad solder results.

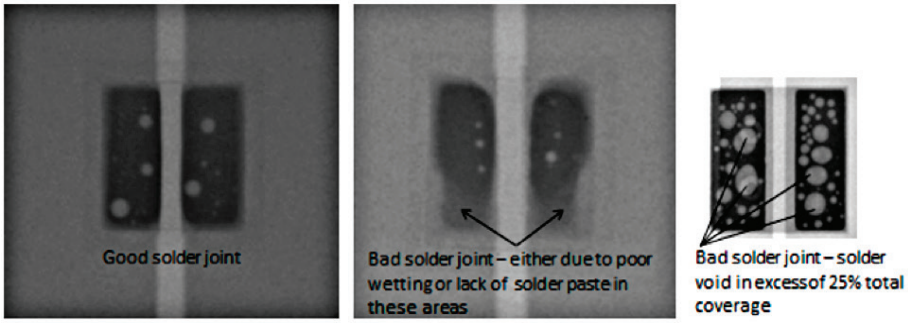


Figure 34. Example of good and bad x-ray result

The maximum acceptable void level should be selected according to the overall thermal condition in the application and desirably not exceed 25% of total pad area. Figure 35 shows the change in thermal resistance junction-to-board-bottom as a function of the void percentage based on simulated data for a LUXEON Neo 0.5mm² on a Cu-IMS board. The board parameters in the simulations are the same as stated in section 4.1, except the bond line thickness. The value of the bond line thickness was taken to be 30/50 µm for the 0% void situation and assumed to increase with increasing void level in a way that the total solder volume remains constant.

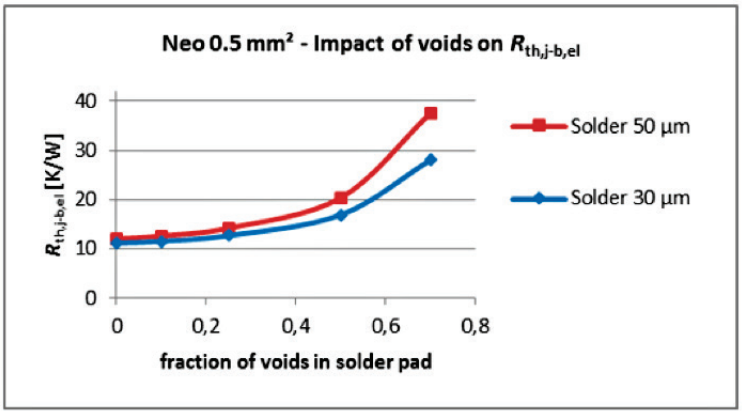


Figure 35. Impact of voids in the solder joint on the thermal resistance

5.11 Reflow Accuracy

For solder mask defined designs, Lumileds facilitated internal tests with shown position accuracy after reflow (see Figure 36 and Table 6). Results may vary based on printed circuit board quality and used assembly process.

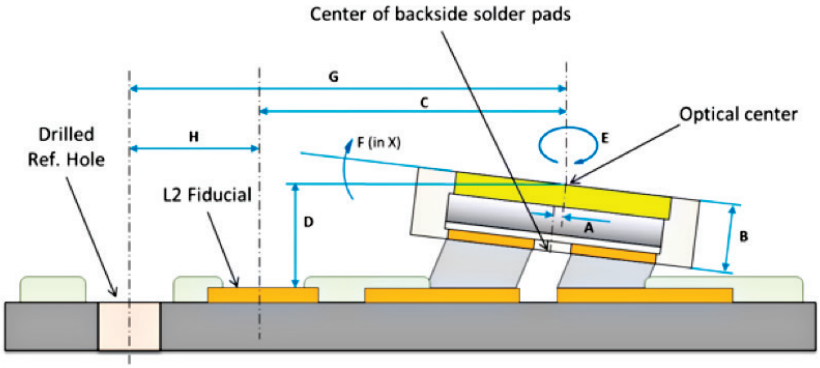


Figure 36. L1 and L2 tolerance definition

Table 6. Dimension and placement tolerances

ITEM	DESCRIPTION	MAXIMUM VALUE (5σ)	TYPICAL VALUE
A	L1: Optical center to back-side metal X/Y	±25 µm	
B	L1: Total thickness Z	±25 µm	
C	L2: Optical center to L2 fiducial, X/Y		±55 µm
D	L2: Optical center to L2 fiducial, Z		±35 µm
E	L2: Optical center to L2 fiducial, Rotation		±5 deg.
F	L2: LED package Tilting to Board		±3 deg. in X ±5 deg. in Y
G	L2: Optical center to L2 Reference Hole		Depending on Board Tolerance H

Note: Typical values given are derived from sample based assembly tests performed at Lumileds and calculated for 5 Sigma.

LED Tilting

Tilting of a LUXEON Neo soldered on a board may increase the position tolerance, especially in Z-direction. Tilting is mainly related to solder thickness and occurs mostly along the long side of pad direction. LUXEON Neo tends to rest either on one or the other side of a board surface (see Figure 37). A good balance between solder mask thickness and print volume should be found in order to lower tilting along the pads. However, solder thickness that is too low will hamper the self-alignment of LUXEON Neo during solder reflow, which is needed for X-Y and rotational alignment on the board. Based on application requirements, a good choice may be to optimize print volume to allow some tilting.

A reduction of the print volume can be done by adjusting the stencil aperture and stencil thickness. A tilting between anode and cathode pad can be affected by unequal print volume or unmatched pad area due to board tolerances.

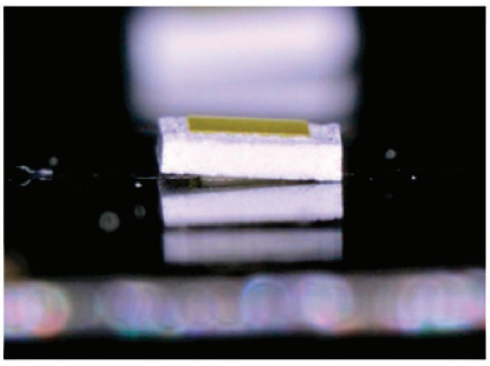


Figure 37. LUXEON Neo soldered to a PCB with high tilting angle

5.12 Electrical Polarity Testing

If a polarity detection is required after assembly at the electrical end-of-line test, the internal eTVS diode must be considered (see Chapter 2.1).

Since this diode is connected in parallel reverse to the LED, an accidently wrong orientated LED will also light up and deliver a voltage reading at the in-circuit tester. Only at nominal drive current will this unit fail within a short time of operation.

In order to do electrical screening for polarity at low current and within a short time, accurate probing and voltage reading is required to detect wrong polarity based on forward voltage. LUXEON Neo LEDs are binned in forward voltage classes, thus, electrical reading of good units should deliver forward voltage in a predictable range; a test current of 30 mA can be used. Units with wrong polarity have noticeably higher voltage reading of >300 mV, more than normal operating at 30 mA test current. Units which were accidently operated at current >10 mA in reverse direction should be scrapped.

5.13 Board Handling and Bending

The LED package handling precaution, as described in section 2.2, must also be applied when handling completed board. Even though this product has a small form factor and is unlikely to cause any problems, forces on the package should be kept to a minimum. Bending of a PCB is a common handling problem typically seen on large boards. A printed circuit board may warp after reflow when layers with different CTE (coefficient of thermal expansion) are applied to the top and bottom of the boards. If the PCB is subsequently secured to a flat surface, a vertical force is applied to the LED package (see Figure 38).

Any deformation by mounting the board and screwing it onto a heatsink by de-paneling, like punching-off or breaking-off, should be kept to minimum. As a general guideline, it should be at most 2mm of vertical deflection for every 90mm of FR4 PCB length. The guideline in Figure 38 should be maintained to prevent the sapphire chip, used in LUXEON Neo, from cracking and causing device failure.

This guideline does not apply to solder joint reliability, as the ability of the solder joint to withstand this stress (elongation) depends on the footprint layout, solder joint thickness, solder voiding and the type of solder paste used.

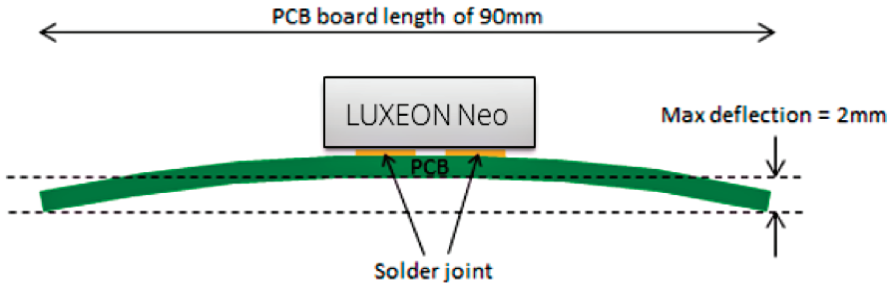


Figure 38. Maximum PCB bending guideline to prevent damage to the LUXEON Neo package

5.14 Packing of Assembled LUXEON Neo Module

Finished boards must be protected against damage during transport. It is recommended to use a customized tray package which is designed to hold the PCBs during transport (see Figure 39).

Here some general rules of best practice tray design:

1. Design the tray to avoid accidently touching the LED by manually taking assemblies out or putting into tray. Ideally, the tray only allows one way to hold the assembly. If there are several ways to put assemblies into the tray or take them out, a strict operator discipline and clear instruction on how to safely handle the assemblies is needed.
2. It must be designed in a way that no force from the tray or packing material is applied to the LED.
3. In a stack of multiple trays, the PCB should also be secured from the top. This can be done by bottom structures of the next tray which is put on top of the stack.
4. The tray should also protect the LED against movement and shaking/vibrations during transport

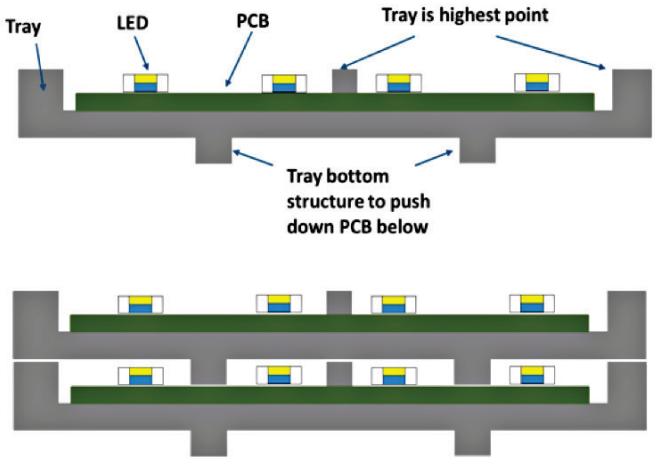


Figure 39. Schematic of a good tray design. The LEDs are protected against movement and no forces are applied to the LEDs

6. Interconnect Reliability

The reliability of board interconnect under thermal cycling and thermal shock condition is mainly determined by thermal expansion of used materials. LUXEON Neo emitter die is made of sapphire which has a low CTE (coefficient of thermal expansion) of ~5-6 ppm. The CTE mismatch between LED and printed circuit board will lead to mechanical stress and cause solder fatigue or solder cracking. To achieve highest possible reliability the CTE of the board material should be similar to the LED. Table 7 shows commonly used materials and their CTE.

Also, the mechanical properties of solder material and solder thickness have an impact on interconnect reliability. Using a ductile material and increasing the bond line thickness will increase solder joint reliability.

Lumileds recommends usage of copper-based board materials in combination with ~40 µm BLT (bond line thickness) and SAC305 solder material to pass the 1,000 cycles TMSK -40/+125 °C test according to JEDEC JESD22-A104E. In most cases, aluminum-based board materials cannot reach this cycle requirement due to a higher CTE mismatch.

Table 7. CTE of common board substrate materials

MATERIAL	COEFFICIENT OF THERMAL EXPANSION (CTE)
Sapphire (LED)	5–6ppm
Solder SAC	19–22ppm
Copper	16.5ppm
FR4	12–17ppm*
Aluminium	23.1ppm
AIN	4ppm
AI203	6–8ppm

* Depending on laminate vendor, prepreg type, and fiber orientation

7. JEDEC Moisture Sensitivity Level

The LUXEON Neo has a JEDEC moisture sensitivity level of 1. This is the highest level offered in the industry and the highest level within the JEDEC J-STD-020D.1 standard. This provides the customer with ease of assembly; the customer no longer needs to be concerned about bake out times and floor life. No bake out time is required for a moisture sensitivity level of 1.

Moisture sensitivity level 1 allows the device to be reflowed three times under the specifications as described in the respective LUXEON Neo datasheets. JEDEC has defined eight levels for moisture sensitivity, as shown in Table 8.

Table 8. CTE of common board substrate materials

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS			
			STANDARD		ACCELERATED EQUIVALENT 1	
	TIME	CONDITIONS	TIME	CONDITIONS	TIME	CONDITIONS
1	Unlimited	≤30 °C / 85% RH	168 hours +5 / -0	85 °C / 85% RH		
2	1 year	≤30 °C / 60% RH	168 hours +5 / -0	85 °C / 60% RH		
2a	4 weeks	≤30 °C / 60% RH	696 hours +5 / -0	30 °C / 60% RH	120 hours +1 / -0	60 °C / 60% RH
3	168 hours	≤30 °C / 60% RH	192 hours +5 / -0	30 °C / 60% RH	40 hours +1 / -0	60 °C / 60% RH
4	72 hours	≤30 °C / 60% RH	96 hours +2 / -0	30 °C / 60% RH	20 hours +5 / -0	60 °C / 60% RH
5	48 hours	≤30 °C / 60% RH	72 hours +2 / -0	30 °C / 60% RH	15 hours +5 / -0	60 °C / 60% RH
5a	24 hours	≤30 °C / 60% RH	48 hours +2 / -0	30 °C / 60% RH	10 hours +5 / -0	60 °C / 60% RH
6	Time on Label (TOL)	≤30 °C / 60% RH	TOL	30 °C / 60% RH		

8. Packaging Considerations—Chemical Compatibility

The LUXEON Neo package contains a silicone overcoat to protect the LED chip and extract the maximum amount of light. As with most silicones used in LED optics, care must be taken to prevent any incompatible chemicals from directly or indirectly reacting with the silicone.

The silicone overcoat in LUXEON Neo is gas permeable. Consequently, oxygen and volatile organic compound (VOC) gas molecules can diffuse into the silicone overcoat. VOCs may originate from adhesives, solder fluxes, conformal coating materials, potting materials and even some of the inks that are used to print the PCBs. Some VOCs and chemicals react with silicone and produce discoloration and surface damage. Other VOCs do not chemically react with the silicone material directly but diffuse into the silicone and oxidize during the presence of heat or light. Regardless of the physical mechanism, both cases may affect the total LED light output. Since silicone permeability increases with temperature, more VOCs may diffuse into and/or evaporate out from the silicone.

Careful consideration must be given to whether LUXEON Neo emitters are enclosed in an "air tight" environment or not. In an "air tight" environment, some VOCs that were introduced during assembly may permeate and remain in the silicone overcoat. Under heat and "blue" light, the VOCs inside the silicone overcoat may partially oxidize and create a silicone discoloration, particularly on the surface of the LED where the flux energy is the highest. In an air rich or "open" air environment, VOCs have a chance to leave the area (driven by the normal air flow). Transferring the devices, which were discolored in the enclosed environment back to "open" air, may allow the oxidized VOCs to diffuse out of the silicone overcoat and may restore the original optical properties of the LED.

Determining suitable threshold limits for the presence of VOCs is very difficult since these limits depend on the type of enclosure used to house the LEDs and the operating temperatures. Also, some VOCs can photo-degrade over time. Table 9 provides a list of commonly used chemicals that should be avoided as they may react with the silicone material. Note that Lumileds does not warrant that this list is exhaustive since it is impossible to determine all chemicals that may affect LED performance.

The chemicals in Table 9 are typically not directly used in the final products that are built around LUXEON Neo LEDs. However, some of these chemicals may be used in intermediate manufacturing steps (e.g. cleaning agents). Consequently, trace amounts of these chemicals may remain on sub-components, such as heatsinks. Lumileds, therefore, recommends the following precautions when designing your application:

1. When designing secondary lenses to be used over an LED, provide a sufficiently large air-pocket and allow for "ventilation" of this air away from the immediate vicinity of the LED.
2. Use mechanical means of attaching lenses and circuit boards as much as possible. When using adhesives, potting compounds and coatings, carefully analyze its material composition and do thorough testing of the entire fixture under High Temperature Over Life (HTOL) conditions.

Table 9. List of commonly used chemicals that may damage the silicone overcoat of LUXEON IR Domed LEDs.

CHEMICAL NAME	TYPICAL USE
Hydrochloric Acid	Acid
Sulfuric Acid	Acid
Nitric Acid	Acid
Acetic Acid	Acid
Sodium Hydroxide	Alkali
Potassium Hydroxide	Alkali
Ammonia	Alkali
MEK (Methyl Ethyl Ketone)	Solvent
MIBK (Methyl Isobutyl Ketone)	Solvent
Toluene	Solvent
Xylene	Solvent
Benzene	Solvent
Gasoline	Solvent
Mineral spirits	Solvent
Dichloromethane	Solvent
Tetracholorometane	Solvent
Castor Oil	Oil
Lard	Oil
Linseed Oil	Oil
Petroleum	Oil
Silicone Oil	Oil
Halogenated Hydrocarbons (containing F, Cl, Br elements)	Misc.
Rosin Flux	Solder Flux
Acrylic Tape	Adhesive

Note: Avoid using any of these chemicals in the housing that contains the LED package.

About Lumileds

Companies developing automotive, mobile, IoT and illumination lighting applications need a partner who can collaborate with them to push the boundaries of light. With over 100 years of inventions and industry firsts, Lumileds is a global lighting solutions company that helps customers around the world deliver differentiated solutions to gain and maintain a competitive edge. As the inventor of Xenon technology, a pioneer in halogen lighting and the leader in high performance LEDs, Lumileds builds innovation, quality and reliability into its technology, products and every customer engagement. Together with its customers, Lumileds is making the world safer, better and more beautiful—with light.

To learn more about our lighting solutions, visit lumileds.com.

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